19-2756; Rev 0; 4/03

±15kV ESD-Protected USB Transceivers

MAX3450E/MAX3451E/MAX3452E

General Description

The MAX3450E/MAX3451E/MAX3452E USB-compliant transceivers interface low-voltage ASICs with USB devices. The devices fully comply with USB 1.1 and USB 2.0 when operating at full (12Mbps) and low (1.5Mbps) speeds. The MAX3450E/MAX3451E/MAX3452E operate with V_L as low as +1.65V, ensuring compatibility with low-voltage ASICs.

The MAX3450E/MAX3451E/MAX3452E feature a logic-selectable suspend mode that reduces current consumption to less than 40µA. Integrated ±15kV ESD protection protects the USB D+ and D- bidirectional bus connections. The MAX3450E is pin compatible with Micrel's MIC2550A. The MAX3451E features an internal 1.5kΩ USB pullup resistor and an enumeration function that allows devices to logically disconnect while plugged in. The MAX3452E provides a push-pull bus-detect (BD) output that asserts high when V_{BUS} is greater than +4.0V.

The MAX3450E/MAX3451E/MAX3452E operate over the -40°C to +85°C extended temperature range and are available in 14-pin TSSOP and 3mm x 3mm 16-pin thin QFN packages.

Applications

PDAs

PC Peripherals

Cellular Telephones

Data Cradles

MP3 Players

Features

- ±15kV ESD Protection on D+ and D-
- USB 1.1 and 2.0 (Low-Speed and Full-Speed) Compliant Transceiver
- Combined VP and VM Inputs/Outputs
- +1.65V to +3.6V V_L Logic Supply Input for Interfacing with Low-Voltage ASICs
- Enumerate Input Function (MAX3451E)
- Powered from Li+ Battery as Low as +3.1V (MAX3450E and MAX3451E)
- V_{BUS} Detection (MAX3452E)
- Pin Compatible with Micrel MIC2550A (MAX3450E)
- Internal D+ or D- Pullup Resistor (MAX3451E)
- No Power-Supply Sequencing Required

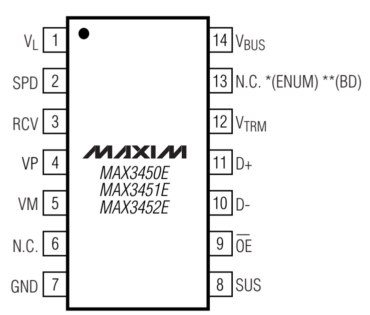
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3450EEUD	-40°C to +85°C	14 TSSOP
MAX3450EETE	-40°C to +85°C	16 Thin QFN
MAX3451EEUD	-40°C to +85°C	14 TSSOP
MAX3451EETE	-40°C to +85°C	16 Thin QFN
MAX3452EEUD	-40°C to +85°C	14 TSSOP
MAX3452EETE	-40°C to +85°C	16 Thin QFN

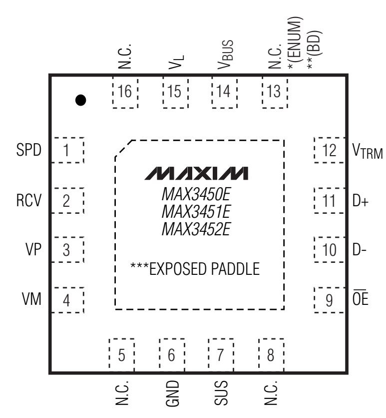
Typical Operating Circuit appears at end of data sheet.

Pin Configurations

TOP VIEW



TSSOP



3mm x 3mm
THIN QFN

*MAX3451E ONLY
**MAX3452E ONLY
***CONNECT EXPOSED PADDLE TO GND OR LEAVE FLOATING

±15kV ESD-Protected USB Transceivers

ABSOLUTE MAXIMUM RATINGS

V_{BUS}, V_L, D+, D- to GND......................................-0.3V to +6.0V
V_{TRM} to GND ....-0.3V to (V_{BUS} + 0.3V)
VP, VM, SUS, SPD, ENUM,
RCV, $\overline{OE}$, BD to GND ....-0.3V to (V_L + 0.3V)
Current (into any pin) ....±15mA
Short-Circuit Current (D+ and D-)..................................±150mA

Continuous Power Dissipation (T_A = +70°C)
14-Pin TSSOP
(derate 9.1mW/°C above +70°C)................................727mW
16-Pin Thin QFN 3mm x 3mm
(derate 14.7mW/°C above +70°C)............................1176mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{BUS} = +4.0V to +5.5V or V_{TRM} = +3.0V to +3.6V, V_L = +1.65V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{BUS} = +5.0V, V_L = +2.5V, and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY INPUTS (V_{BUS}, V_{TRM}, V_L)							
Regulated Supply Voltage Output	V_{TRM}	Internal regulator		3.0	3.3	3.6	V
Operating Supply Current	I_{VBUS}	Full-speed transmitting/receiving at 12Mbps, C_L = 50pF on D+ and D- (Note 2)			5	10	mA
Operating V_L Supply Current	I_{VL}	Full-speed transmitting/receiving at 12Mbps (Note 2)			0.4	1	mA
Full-Speed Idle and SE0 Supply Current	$I_{VBUS(IDLE)}$	Full-speed idle: V_{D+} > 2.7V, V_{D-} < 0.3V			250	350	µA
		SE0: V_{D+} < 0.3V, V_{D-} < 0.3V			250	350	
Static V_L Supply Current	$I_{VL(STATIC)}$	Full-speed idle, SE0, or suspend mode	MAX3450E, MAX3451E			5	µA
			MAX3452E			10	
Suspend Supply Current	$I_{VBUS(SUSP)}$	VM = VP = open, SUS = $\overline{OE}$ = high	MAX3450E, MAX3451E (ENUM = low)			35	µA
			MAX3452E			40	
Disable-Mode Supply Current	$I_{VBUS(DIS)}$	V_L = GND or open				20	µA
Sharing-Mode V_L Supply Current	$I_{VL(SHARING)}$	V_{BUS} = GND or open, $\overline{OE}$ = low, VP = low or high, VM = low or high, SUS = high	MAX3450E, MAX3451E			5	µA
			MAX3452E			20	
D+/D- Sharing-Mode Load Current	$I_{D\_(SHARING)}$	V_{BUS} = GND or open, $V_{D\_}$ = 0 or +5.5V				20	µA
D+/D- Disable-Mode Load Current	$I_{D\_(DIS)}$	V_L = GND or open, $V_{D\_}$ = 0 or +5.5V				5	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{BUS} = +4.0V to +5.5V or V_{TRM} = +3.0V to +3.6V, V_L = +1.65V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{BUS} = +5.0V, V_L = +2.5V, and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB Power-Supply Detection Threshold	V_{TH_VBUS}	MAX3450E/MAX3451E, supply lost			0.8	V
		MAX3450E/MAX3451E, supply present (Note 3)	3.6			
		MAX3452E, supply lost			3.6	
		MAX3452E, supply present	4.0			
USB Power-Supply Detection Hysteresis	V_{HYST_VBUS}	MAX3450E/MAX3451E		75		mV
		MAX3452E		40		
V_L Power-Supply Detection Threshold	V_{TH_VL}			0.85		V
DIGITAL INPUTS/OUTPUTS (VP, VM, RCV, SUS, $\overline{OE}$, SPD, BD, ENUM)						
Input Voltage Low	V_{IL}	VM, VP, SUS, SPD, ENUM, $\overline{OE}$			0.3 x V_L	V
Input Voltage High	V_{IH}	VM, VP, SUS, SPD, ENUM, $\overline{OE}$	0.7 x V_L			V
Output Voltage Low	V_{OL}	VM, VP, RCV, BD, I_{OL} = +2mA			0.4	V
Output Voltage High	V_{OH}	VM, VP, RCV, BD, I_{OH} = -2mA	V_L - 0.4			V
Input Leakage Current	I_{LKG}		-1		+1	µA
Input Capacitance	C_{IN}	Measured from input to GND		10		pF
ANALOG INPUTS/OUTPUTS (D+, D-)						
Differential Input Sensitivity	V_{ID}	$\lvert V_{D+} - V_{D-} \rvert$	0.2			V
Differential Common-Mode Voltage	V_{CM}	Includes V_{ID} range	0.8		2.5	V
Single-Ended Input Low Voltage	V_{ILSE}				0.8	V
Single-Ended Input High Voltage	V_{IHSE}		2.0			V
Hysteresis	V_{HYST}			250		mV
Output Voltage Low	V_{OLD}	R_L = 1.5kΩ to +3.6V			0.3	V
Output Voltage High	V_{OHD}	R_L = 15kΩ to GND	2.8		3.6	V
Off-State Leakage Current	I_{LZ}		-1		+1	µA
Transceiver Capacitance	C_{IND}	Measured from D_ to GND		20		pF
Driver Output Impedance	Z_{DRV}	Steady-state drive	4.0		19.5	Ω
Input Impedance	Z_{IN}	Driver off	10			MΩ
Internal Pullup Resistance	R_{PULLUP}	I_{LOAD} = 500µA (MAX3451E) (Note 4)	1.425		1.575	kΩ
ESD PROTECTION (D+, D-)						
Human Body Model				±15		kV
IEC 1000-4-2 Contact Discharge				±8		kV

TIMING CHARACTERISTICS

(V_{BUS} = +4.0V to +5.5V or V_{TRM} = +3.0V to +3.6V, V_L = +1.65V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{BUS} = +5V, V_L = +2.5V, and T_A = +25°C.) (Note 1)

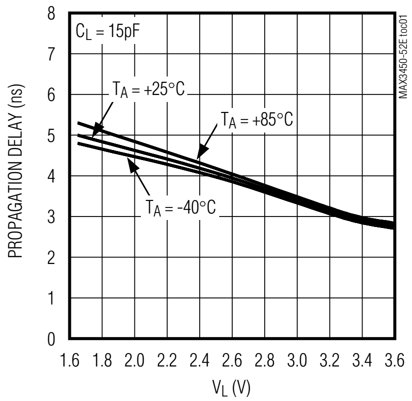
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER CHARACTERISTICS (FULL-SPEED MODE, C_L = 50pF)						
Rise Time	t_{FR}	10% to 90% of $\|V_{OHD}$ - $V_{OLD}\|$, Figures 1, 6	4		20	ns
Fall Time	t_{FF}	90% to 10% of $\|V_{OHD}$ - $V_{OLD}\|$, Figures 1, 6	4		20	ns
Rise-/Fall-Time Matching (Note 2)	t_{FR}/t_{FF}	Excluding the first transition from idle state, (Figures 1, 6)	90		110	%
Output-Signal Crossover Voltage (Note 2)	V_{CRS_F}	Excluding the first transition from idle state, (Figures 2, 6)	1.3		2.0	V
Driver Propagation Delay (Figures 2, 6)	t_{PLH_DRV}	Low-to-high transition			18	ns
	t_{PHL_DRV}	High-to-low transition			18	
Driver Disable Delay (Figure 3)	t_{PHZ_DRV}	High-to-off transition			20	ns
	t_{PLZ_DRV}	Low-to-off transition			20	
Driver Enable Delay (Figure 3)	t_{PZH_DRV}	Off-to-high transition			20	ns
	t_{PZL_DRV}	Off-to-low transition			20	
DRIVER CHARACTERISTICS (LOW-SPEED MODE, C_L = 200pF TO 600pF)						
Rise Time	t_{LR}	10% to 90% of $\|V_{OHD}$ - $V_{OLD}\|$, Figures 1, 6	75		300	ns
Fall Time	t_{LF}	90% to 10% of $\|V_{OHD}$ - $V_{OLD}\|$, Figures 1, 6	75		300	ns
Rise-/Fall-Time Matching	t_{LR}/t_{LF}	Excluding the first transition from idle state, Figures 1, 6	80		125	%
Output-Signal Crossover Voltage	V_{CRS_L}	Excluding the first transition from idle state, Figures 2, 6	1.3		2.0	V
RECEIVER CHARACTERISTICS (C_L = 15pF)						
Differential Receiver Propagation Delay, Figures 4, 6	t_{PLH_RCV}	Low-to-high transition			22	ns
	t_{PHL_RCV}	High-to-low transition			22	
Single-Ended Receiver Propagation Delay, Figures 4, 6	t_{PLH_SE}	Low-to-high transition			12	ns
	t_{PHL_SE}	High-to-low transition			12	
Single-Ended Receiver Disable Delay, Figure 5	t_{PHZ_SE}	High-to-off transition			15	ns
	t_{PLZ_SE}	Low-to-off transition			15	
Single-Ended Receiver Enable Delay, Figure 5	t_{PZH_SE}	Off-to-high transition			15	ns
	t_{PZL_SE}	Off-to-low transition			15	

Note 1: Parameters are 100% production tested at +25°C, limits over temperature are guaranteed by design.
Note 2: Guaranteed by design, not production tested.
Note 3: Production tested to +2.7V for $V_L \leq$ +3.0V.
Note 4: Including external 24.3Ω series resistor.

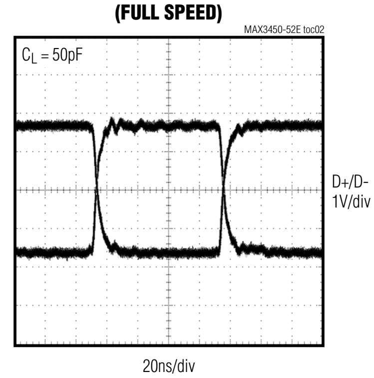
Typical Operating Characteristics

(V_{BUS} = +5.0V, V_L = +3.3V, T_A = +25°C, unless otherwise noted.)

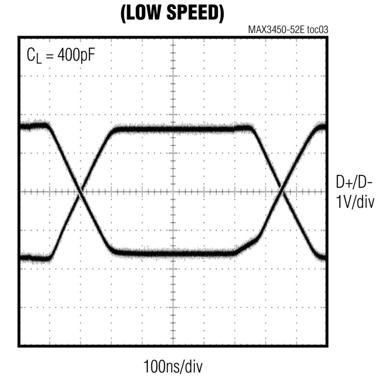
SINGLE-ENDED RECEIVER PROPAGATION DELAY vs. V_L



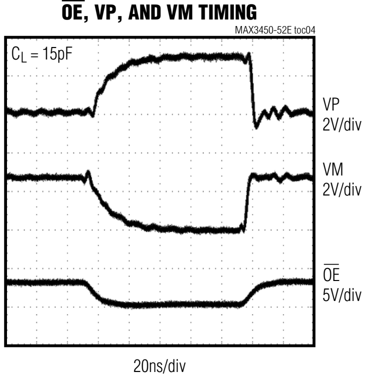
RISE-/FALL-TIME MATCHING (FULL SPEED)



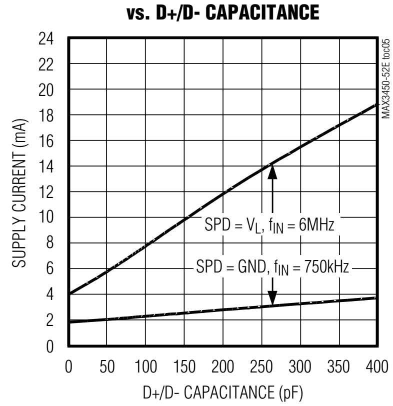
RISE-/FALL-TIME MATCHING (LOW SPEED)



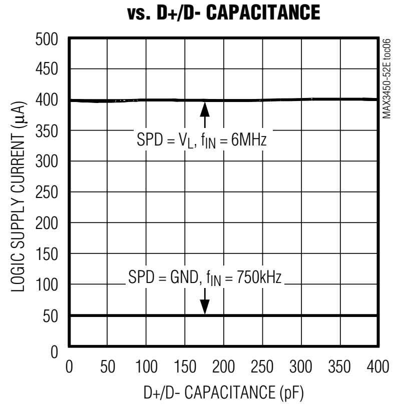
$\overline{OE}$, VP, AND VM TIMING



SUPPLY CURRENT vs. D+/D- CAPACITANCE



LOGIC SUPPLY CURRENT vs. D+/D- CAPACITANCE

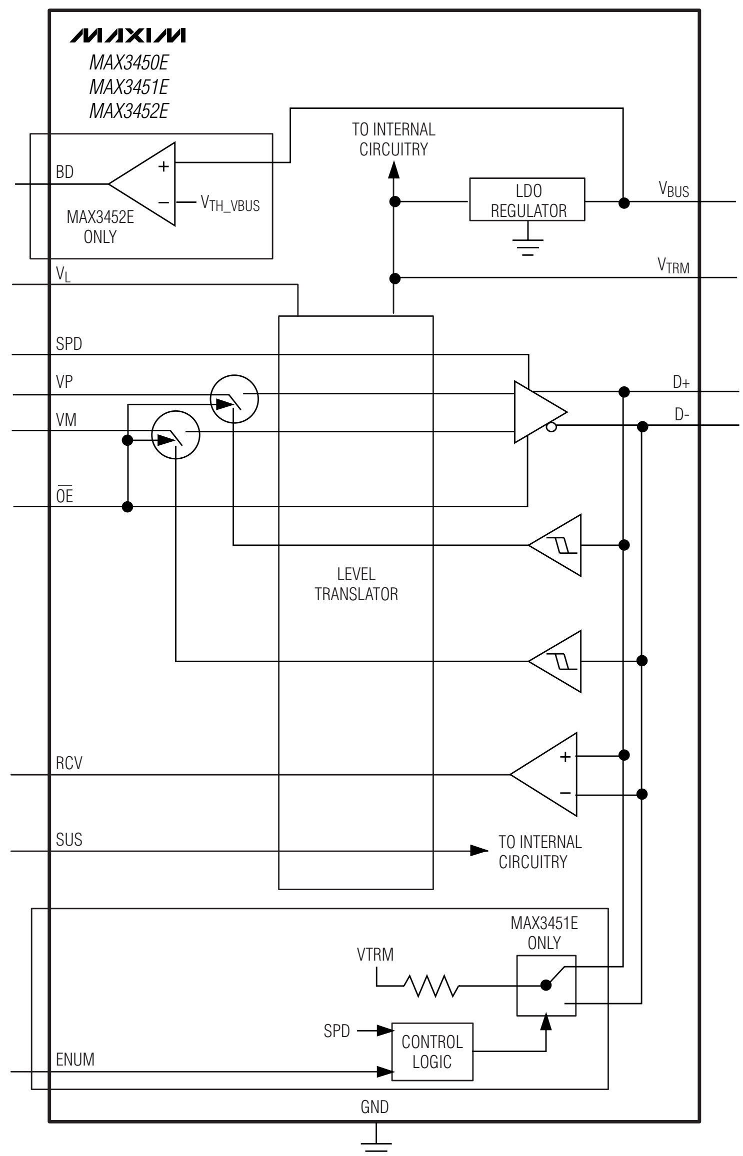


±15kV ESD-Protected USB Transceivers

Pin Description

PIN		NAME	FUNCTION
TSSOP	QFN		
1	15	V_L	Digital I/O Connections Logic Supply. Connect a +1.65V to +3.6V supply to V_L. Bypass V_L to GND with a 0.1µF ceramic capacitor.
2	1	SPD	Speed-Selector Input. Connect SPD to GND to select the low-speed data rate (1.5Mbps). Connect SPD to V_L to select the full-speed data rate (12Mbps).
3	2	RCV	Differential-Receiver Output. RCV responds to the differential input on D+ and D- (Tables 3 and 4). RCV asserts low if SUS = V_L.
4	3	VP	Receiver Output/Driver Input. VP functions as a receiver output when $\overline{OE}$ = V_L. VP duplicates D+ when receiving. VP functions as a driver input when $\overline{OE}$ = GND.
5	4	VM	Receiver Output/Driver Input. VM functions as a receiver output when $\overline{OE}$ = V_L. VM duplicates D- when receiving. VM functions as a driver input when $\overline{OE}$ = GND.
6	5, 8, 16	N.C.	No Connection. Not internally connected.
7	6	GND	Ground
8	7	SUS	Suspend Input. Drive SUS low for normal operation. Drive SUS high to put the MAX3450E/MAX3451E/MAX3452E into suspend mode. RCV asserts low in suspend mode. VP and VM remain active in suspend mode.
9	9	$\overline{OE}$	Output Enable. Drive $\overline{OE}$ to GND to enable the transmitter outputs. Drive $\overline{OE}$ to V_L to disable the transmitter outputs. $\overline{OE}$ also controls the I/O direction of VP and VM (Tables 3 and 4).
10	10	D-	USB Input/Output. For $\overline{OE}$ = GND, D- functions as a USB output, with VM providing the input signal. For $\overline{OE}$ = V_L, D- functions as a USB input, with VM functioning as a single-ended receiver output. Connect a 1.5kΩ resistor from D- to V_{TRM} for low-speed (1.5Mbps) operation (MAX3450E and MAX3452E).
11	11	D+	USB Input/Output. For $\overline{OE}$ = GND, D+ functions as a USB output, with VP providing the input signal. For $\overline{OE}$ = V_L, D+ functions as a USB input, with VP functioning as a single-ended receiver output. Connect a 1.5kΩ resistor from D+ to V_{TRM} for full-speed (12Mbps) operation (MAX3450E and MAX3452E).
12	12	V_{TRM}	Internal Regulator Output. V_{TRM} provides a regulated +3.3V output. Bypass V_{TRM} to GND with a 1µF (min) ceramic capacitor as close to the device as possible. V_{TRM} normally derives power from V_{BUS}. Alternatively, drive V_{TRM} directly with a +3.3V ±10% supply (MAX3450E and MAX3451E). V_{TRM} provides power to internal circuitry and should not be used to power external circuitry.
13	13	N.C.	No Connection. Not internally connected (MAX3450E).
		ENUM	Enumerate Function Selection Input (MAX3451E). Drive ENUM to V_L to connect the internal 1.5kΩ resistor between V_{TRM} and D+ or D-, depending on the SPD state. Drive ENUM to GND to disconnect the internal 1.5kΩ resistor. For SPD = V_L, the 1.5kΩ pullup resistor connects to D+. For SPD = GND, the 1.5kΩ pullup resistor connects to D-.
		BD	Bus-Detection Output (MAX3452E). The push-pull BD output asserts low and the device enters sharing mode if $V_{BUS} < +3.6V$. BD asserts high if $V_{BUS} > +4.0V$.
14	14	V_{BUS}	USB Power-Supply Input. Connect a +4.0V to +5.5V power supply to V_{BUS}. V_{BUS} provides power to the internal linear regulator. Bypass V_{BUS} to GND with a 0.1µF ceramic capacitor as close to the device as possible. Connect V_{BUS} and V_{TRM} together when powering the MAX3450E or MAX3451E with an external power supply (+3.3V ±10%).

Functional Diagram



Detailed Description

The MAX3450E/MAX3451E/MAX3452E USB-compliant transceivers convert single-ended or differential logic-level signals to USB signals and USB signals to single-ended or differential logic-level signals. The devices fully comply with USB 1.1, as well as USB 2.0 at full- (12Mbps) and low-speed (1.5Mbps) operation. The MAX3450E/MAX3451E/MAX3452E operate with V_L as low as +1.65V, ensuring compatibility with low-voltage ASICs.

The MAX3450E/MAX3451E/MAX3452E derive power from the USB host (V_{BUS}) or from a single-cell Li+ battery (MAX3450E and MAX3451E) connected to V_{BUS}. The MAX3450E/MAX3451E/MAX3452E meet the USB physical-layer specifications for logic-level supply voltages (V_L) from +1.65V to +3.6V. Integrated ±15kV ESD protection protects the D+ and D- USB I/O ports.

The MAX3451E features an enumerate function providing an internal 1.5kΩ pullup resistor to V_{TRM}. The enumerate function disconnects the 1.5kΩ pullup resistor, allowing the MAX3451E to simulate a bus disconnect while powered and connected to the USB cable. The MAX3450E is pin-for-pin compatible with Micrel's MIC2550A. The MAX3452E features a BD output that asserts high if V_{BUS} is greater than +4.0V. BD asserts low if V_{BUS} is less than +3.6V. The MAX3450E and MAX3452E require external pullup resistors from either D+ or D- to V_{TRM} to set the bus speed.

Applications Information

Power-Supply Configurations

Normal Operating Mode

Connect V_L and V_{BUS} to system power supplies (Table 1). Connect V_L to a +1.65V to +3.6V supply. Connect V_{BUS} to a +4.0V to +5.5V supply. Alternatively, the MAX3450E and MAX3451E can derive power from a single Li+ battery. Connect the battery to V_{BUS}. V_{TRM} remains above +3.0V for V_{BUS} as low as +3.1V.

Additionally, the MAX3450E and MAX3451E can derive power from a +3.3V ±10% voltage regulator. Connect V_{BUS} and V_{TRM} to an external +3.3V voltage regulator. V_{BUS} no longer consumes current to power the internal linear regulator in this configuration.

Disable Mode

Connect V_{BUS} to a system power supply and leave V_L unconnected or connect to GND. D+ and D- enter a tri-state mode and V_{BUS} (or V_{BUS} and V_{TRM}) consumes less than 20µA of supply current. D+ and D- withstand external signals up to +5.5V in disable mode (Table 2).

Sharing Mode

Connect V_L to a system power supply and leave V_{BUS} (or V_{BUS} and V_{TRM}) unconnected or connect to GND. D+ and D- enter a tri-state mode, allowing other circuitry to share the USB D+ and D- lines, and V_L consumes less than 20µA of supply current. D+ and D- withstand external signals up to +5.5V in sharing mode (Table 2).

Table 1. Power-Supply Configurations

V_{BUS} (V)	V_{TRM} (V)	V_L (V)	CONFIGURATION	NOTES
+4.0 to +5.5	+3.3 output	+1.65 to +3.6	Normal mode	—
+3.1 to +4.5	+3.3 output	+1.65 to +3.6	Battery supply	MAX3450E, MAX3451E
+3.0 to +3.6	+3.0 to +3.6 input	+1.65 to +3.6	Voltage regulator supply	MAX3450E, MAX3451E
GND or floating	Output	+1.65 to +3.6	Sharing mode	Table 2
+3.0 to +5.5	V_{BUS}	GND or floating	Disable mode	Table 2

Table 2. Disable-Mode and Sharing-Mode Connections

INPUTS/OUTPUTS	DISABLE MODE	SHARING MODE
V_{BUS}/V_{TRM}	• +5V input/+3.3V output • +3.3V input/+3.3V input (MAX3450E and MAX3451E) • +3.7V input/+3.3V output (MAX3450E and MAX3451E)	• Floating or connected to GND (MAX3450E and MAX3451) • < +3.6V (MAX3452E)
V_L	Floating or connected to GND	+1.65V to +3.6V input
D+ and D-	High impedance	High impedance
VP and VM	Invalid*	High impedance for $\overline{OE}$ = low
		High for $\overline{OE}$ = high
RCV	Invalid*	Undefined**
SPD, SUS, $\overline{OE}$, ENUM (MAX3451E)	High impedance	High impedance
BD (MAX3452E)	Invalid*	Low

*High impedance or low
**High or low

Device Control

$\overline{OE}$

$\overline{OE}$ controls the direction of communication. Drive $\overline{OE}$ low to transfer data from the logic side to the USB side. For $\overline{OE}$ = low, VP and VM serve as differential driver inputs to the USB transmitter.

Drive $\overline{OE}$ high to transfer data from the USB side to the logic side. For $\overline{OE}$ = high, VP and VM serve as single-ended receiver outputs from the USB inputs (D+ and D-). RCV serves as a differential receiver output, regardless of the state of $\overline{OE}$.

ENUM (MAX3451E)

The MAX3451E features an enumerate function that allows software control of USB enumeration. USB protocol requires a 1.5kΩ pullup resistor to D+ or D- to indicate the transmission speed to the host (see the *SPD* section). The MAX3451E provides an internal 1.5kΩ pullup resistor. Remove the pullup resistor from the circuit to simulate a device disconnect from the USB. Drive ENUM low to disconnect the internal pullup resistor. Drive ENUM high to connect the internal pullup resistor. The SPD state determines whether the pullup resistor connects to D+ or D-. For ENUM = high, the internal 1.5kΩ pullup resistor connects to D+ when SPD = V_L (full speed) or to D- when SPD = GND (low speed).

SPD

SPD sets the transceiver speed. Connect SPD to GND to select the low-speed data rate (1.5Mbps). Connect SPD to V_L to select the full-speed data rate (12Mbps).

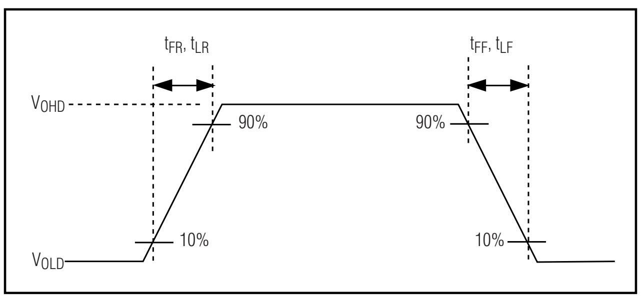


Figure 1. Rise and Fall Times

SUS

The SUS state determines whether the MAX3450E/MAX3451E/MAX3452E operate in normal mode or in suspend mode. Connect SUS to GND to enable normal operation. Drive SUS high to enable suspend mode. RCV asserts low and VP and VM remain active in suspend mode (Tables 3 and 4). Supply current decreases in suspend mode (see the *Electrical Characteristics*).

Table 3a. Transmit Truth Table ($\overline{OE}$ = 0, SUS = 0)

INPUTS		OUTPUTS			OUTPUT STATE
VP	VM	D+	D-	RCV	
0	0	0	0	X	SE0
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X	Undefined

X = Undefined.

Table 3b. Transmit Truth Table ($\overline{OE}$ = 0, SUS = 1)

INPUTS		OUTPUTS			OUTPUT STATE
VP	VM	D+	D-	RCV	
0	0	0	0	0	SE0
0	1	0	1	0	Logic 0
1	0	1	0	0	Logic 1
1	1	1	1	0	Undefined

Table 4a. Receive Truth Table ($\overline{OE}$ = 1 and SUS = 0)

INPUTS		OUTPUTS			OUTPUT STATE
D+	D-	VP	VM	RCV	
0	0	0	0	X	SE0
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X	Undefined

X = Undefined.

Table 4b. Receive Truth Table ($\overline{OE}$ = 1 and SUS = 1)

INPUTS		OUTPUTS			OUTPUT STATE
D+	D-	VP	VM	RCV	
0	0	0	0	0	SE0
0	1	0	1	0	Logic 0
1	0	1	0	0	Logic 1
1	1	1	1	0	Undefined

BD (MAX3452E)

The push-pull bus detect (BD) output monitors V_{BUS} and asserts high if V_{BUS} is greater than +4.0V. BD asserts low if V_{BUS} is less than +3.6V and the MAX3452E enters sharing mode (Table 2).

V_{TRM}

An internal linear regulator generates the V_{TRM} voltage (+3.3V typ). V_{TRM} derives power from V_{BUS} (see the *Power-Supply Configurations* section). V_{TRM} powers the internal portions of the USB circuitry. Bypass V_{TRM} to GND with a 1µF ceramic capacitor as close to the device as possible. Do not use V_{TRM} to provide power to external circuitry.

D+ and D-

D+ and D- serve as bidirectional bus connections and are ESD protected to ±15kV (Human Body Model). For $\overline{OE}$ = low, D+ and D- serve as transmitter outputs. For $\overline{OE}$ = high, D+ and D- serve as receiver inputs. The SPD state determines the slew rate of D+ and D-.

V_{BUS}

For most applications, V_{BUS} connects to the V_{BUS} terminal on the USB connector. V_{BUS} can also connect to an external supply as low as +3.1V (MAX3450E and MAX3451E). See the *Power-Supply Configurations* section. Drive V_{BUS} low to enable sharing mode. Bypass V_{BUS} to GND with a 0.1µF ceramic capacitor as close to the device as possible.

External Components

External Resistors

Proper USB operation requires two external resistors, each 24.3Ω ±1%, 1/8W (or greater). Install one resistor in series between D+ of the MAX3450E/MAX3451E/MAX3452E and D+ on the USB connector. Install the other resistor in series between D- of the MAX3450E/MAX3451E/MAX3452E and D- on the USB connector (see the *Typical Operating Circuit*).

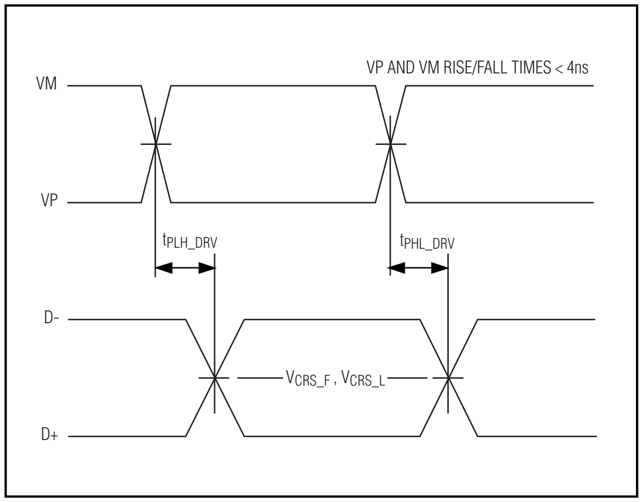


Figure 2. Timing of VP and VM to D+ and D-

External Capacitors

The MAX3450E/MAX3451E/MAX3452E require three external capacitors for proper operation. Bypass V_L to GND with a 0.1µF ceramic capacitor. Bypass V_{BUS} to GND with a 0.1µF ceramic capacitor. Bypass V_{TRM} to GND with a 1µF (min) ceramic capacitor. Install all capacitors as close to the device as possible.

Data Transfer

Transmitting Data to the USB

The MAX3450E/MAX3451E/MAX3452E transmit data to the USB differentially on D+ and D-. VP and VM serve as differential input signals to the driver (Tables 3a and 3b).

Note: During low-speed suspend mode, the slew-rate control circuit consumes less current than normal. This results in a much lower slew rate than during normal operation. The reduced slew rate lengthens the effective propogation time of driving the K state from VP/VM to D+/D- that a peripheral uses to indicate remote wake-up. Applications doing remote wake-up from the low-speed suspend state may need to compensate for this.

Receiving Data from the USB

To receive data from the USB, drive $\overline{OE}$ high and SUS low. Differential data received by D+ and D- appears as a differential logic signal at RCV. Single-ended receivers on D+ and D- drive VP and VM, respectively.

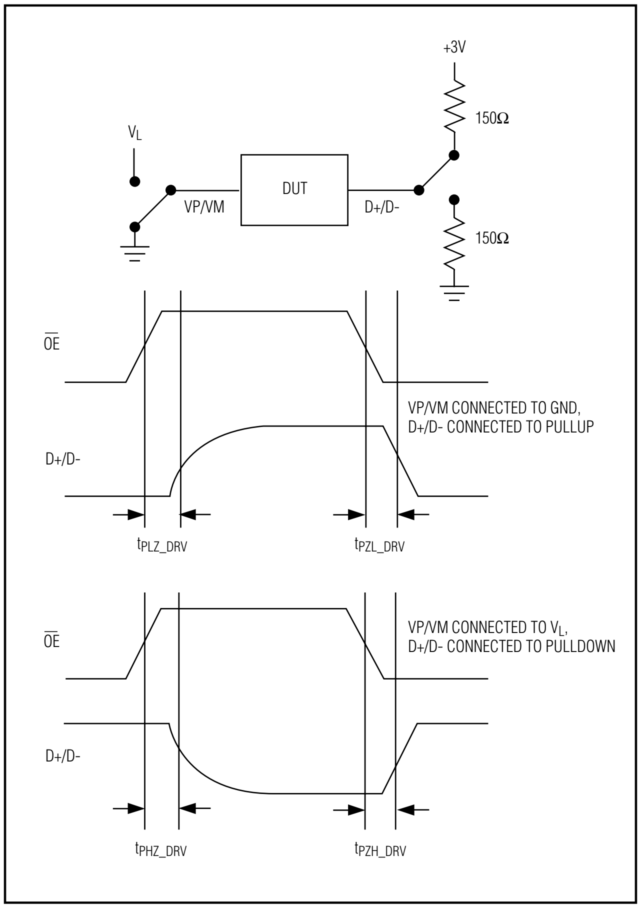


Figure 3. Enable and Disable Timing, Driver

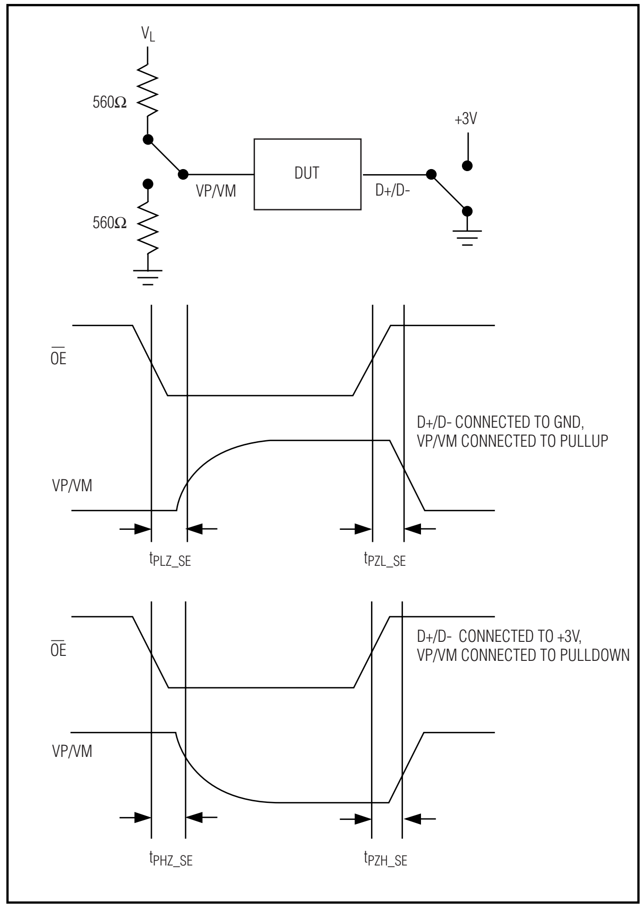


Figure 5. Enable and Disable Timing, Receiver

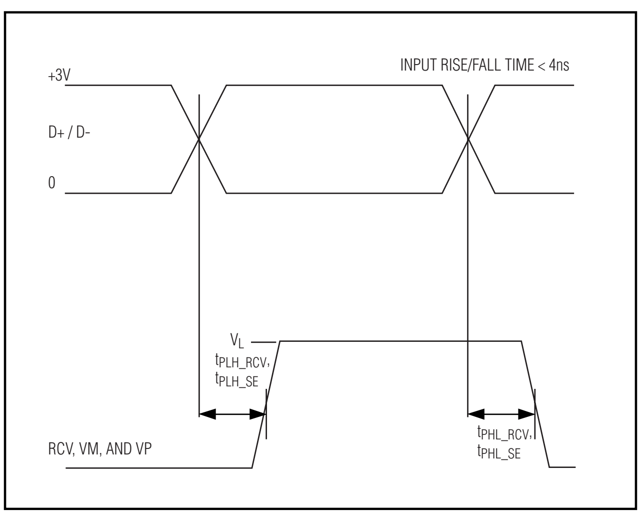


Figure 4. Timing of D+ and D- to RCV, VM, and VP

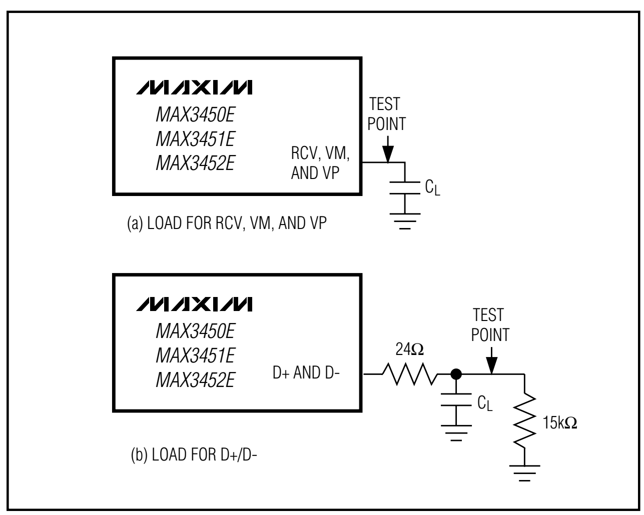


Figure 6. Test Circuits

ESD Protection

D+ and D- possess extra protection against static electricity to protect the devices up to ±15kV. The ESD structures withstand high ESD in all operating modes: normal operation, suspend mode, and powered down. D+ and D- provide protection to the following limits:

- ±15kV using the Human Body Model
- ±8kV using the Contact Discharge method specified in IEC 1000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 7 shows the Human Body Model and Figure 8 shows the current waveform generated when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which then discharges into the test device through a 1.5kΩ resistor.

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The major difference between tests done using the Human Body Model and IEC 1000-4-2 is a higher peak current in IEC 1000-4-2, due to lower series resistance. Hence, the ESD withstand voltage measured to IEC 1000-4-2 generally is lower than that measured using the Human Body Model. Figure 9 shows the IEC 1000-4-2 model. The Contact Discharge method connects the probe to the device before the probe is charged.

Machine Model

The Machine Model for ESD tests all connections using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. All pins require this protection during manufacturing, not just inputs and outputs. After PC board assembly, the Machine Model is less relevant to I/O ports.

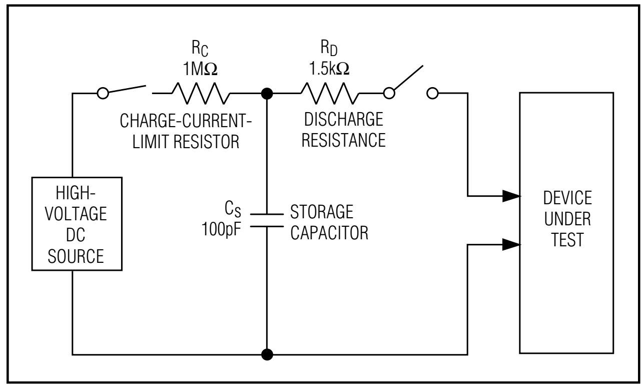


Figure 7. Human Body ESD Test Models

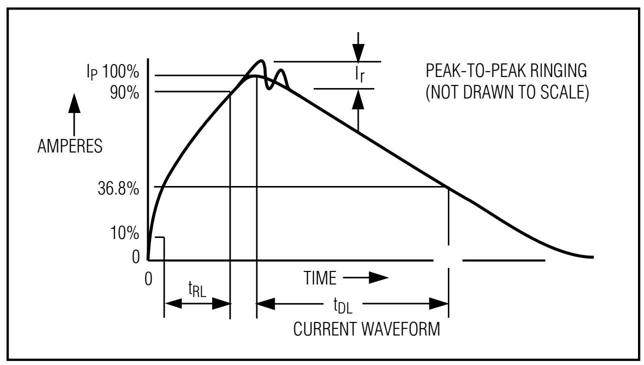


Figure 8. Human Body Model Current Waveform

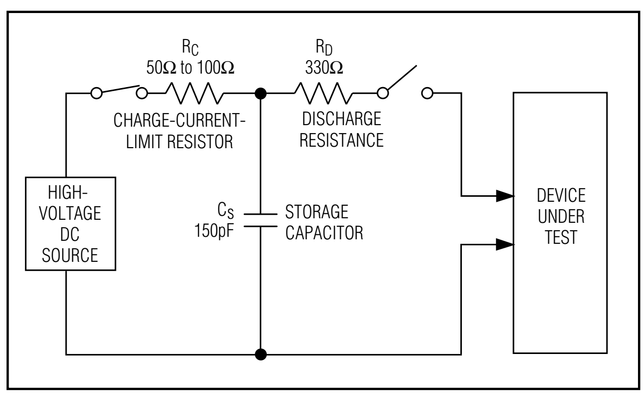
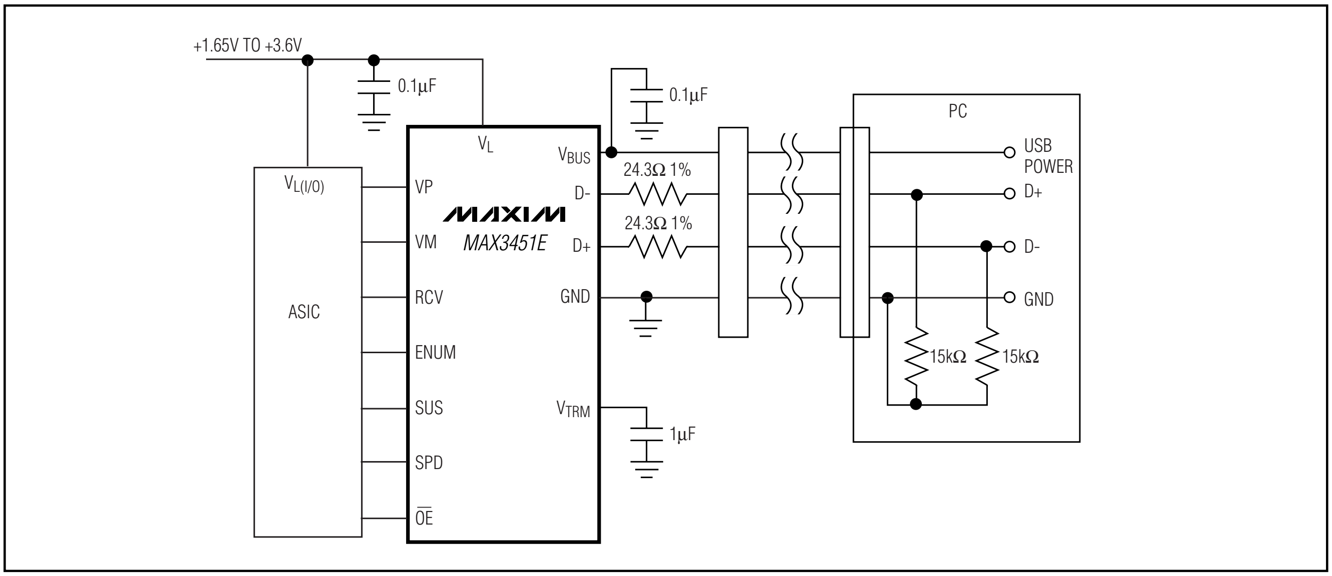


Figure 9. IEC 1000-4-2 ESD Test Model

Typical Operating Circuit



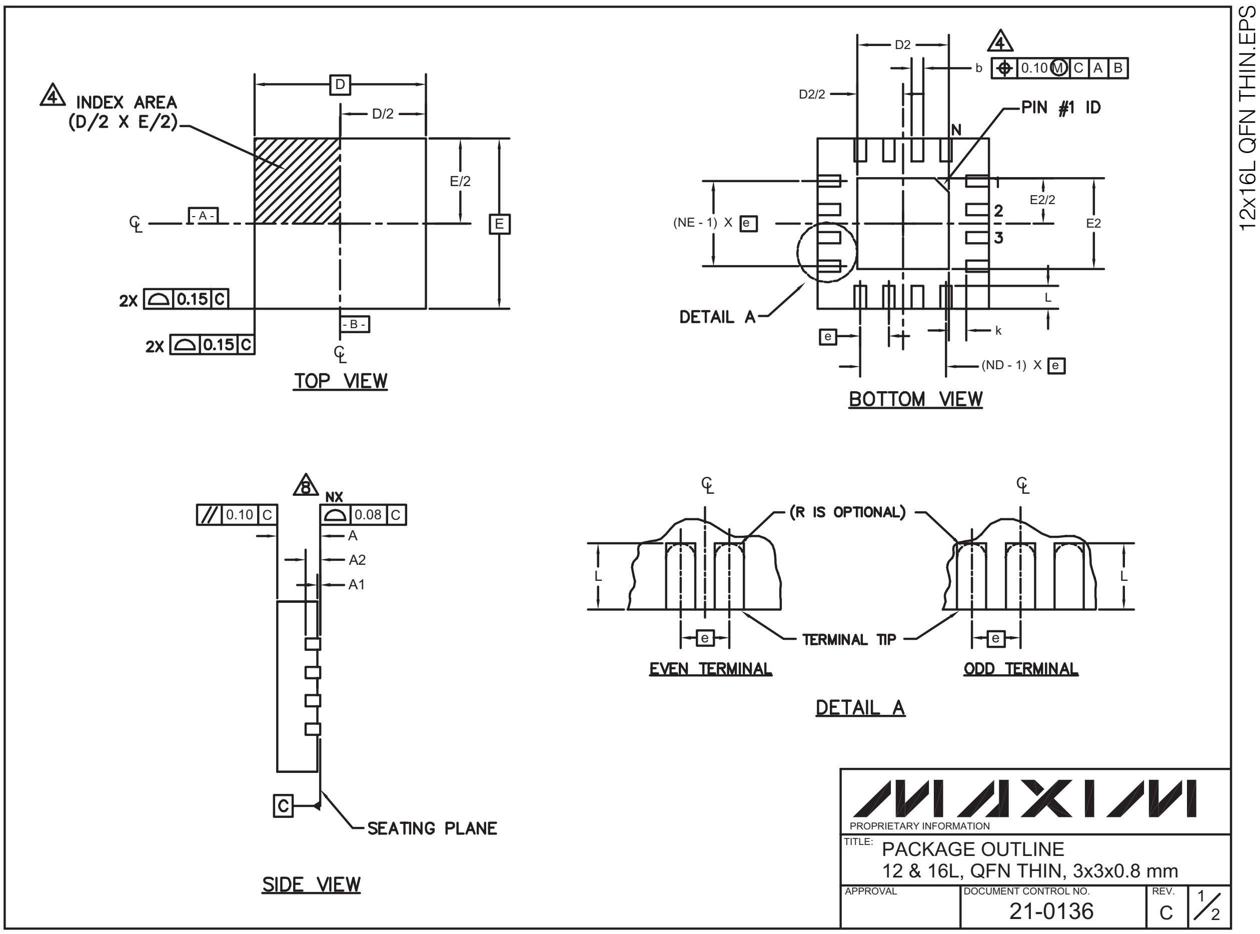
Chip Information

TRANSISTOR COUNT: 873

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PKG	12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	-

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.

MAXIM

PROPRIETARY INFORMATION

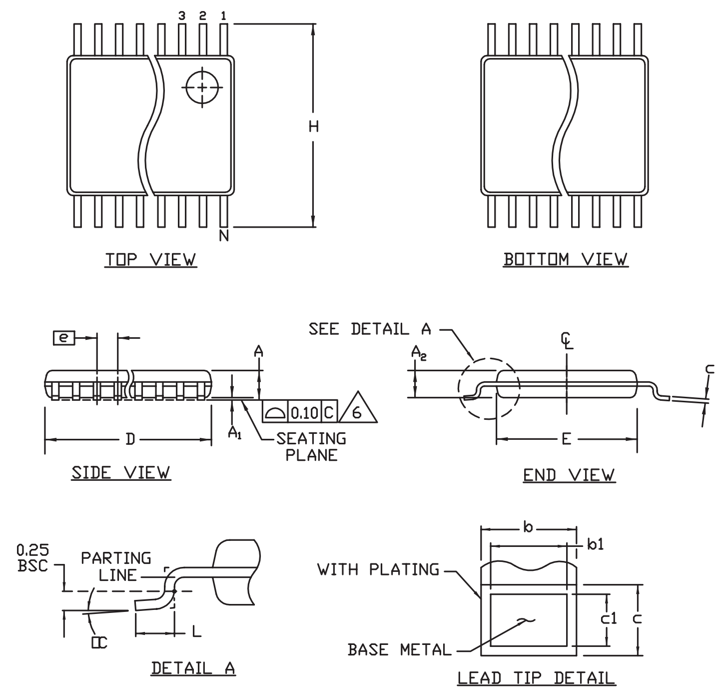
TITLE: PACKAGE OUTLINE
12 & 16L, QFN THIN, 3x3x0.8 mm

APPROVAL | DOCUMENT CONTROL NO. 21-0136 | REV. C | 2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10		.043
A1	0.05	0.15	.002	.006
A2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1